Applying a Drain Voltage to an NMOS Device

Say we apply a voltage at the **gate** of an NMOS device that is sufficiently large to **induce** a conducting channel (i.e., $v_{GS} - V_t > 0$).

Now, say that we additionally place a voltage at the NMOS **drain** electrode, such that:

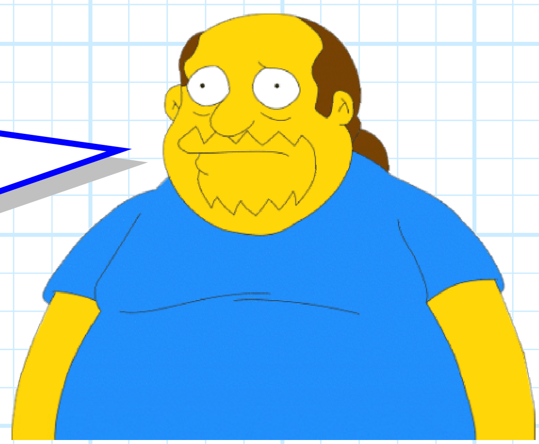
$$v_{DS} > 0$$

where:

$$v_{DS} = v_D - v_S \doteq \text{Drain-to-Source Voltage}$$

Now guess what happens—**current** begins to flow through the **induced channel**!

Q: *Current! I thought current could* ***not*** *flow because of the two p-n junctions in the NMOS device!*



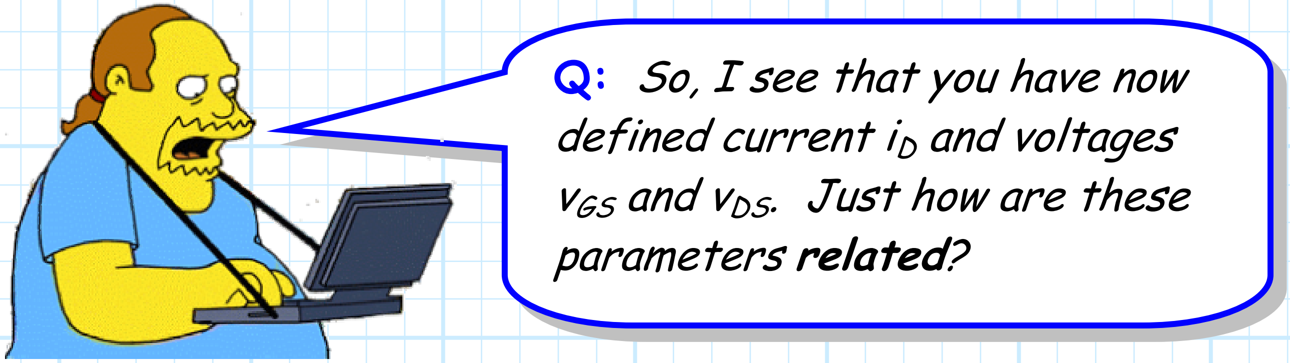
A: Remember, that was **before** we applied a sufficient **gate voltage**. With this voltage applied, an *n*-type channel is **induced**, forming a **conducting channel** from drain to source!

Recall that because of the SiO_2 layer, the gate current is **zero** (i.e., $i_G = 0$).

Thus, all current **entering the drain** will **exit the source**. We therefore conclude that:

$$i_S = i_D$$

As a result, we refer to the channel current for NMOS devices as simply the **drain current** i_D.

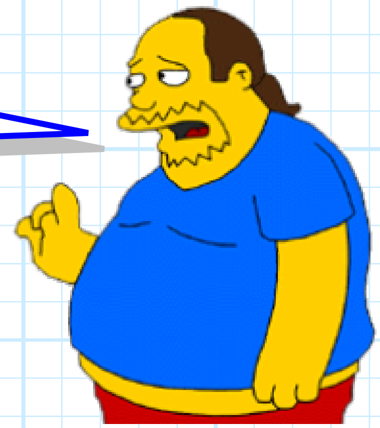


A: First, we find that an **increasing** v_{GS} or, more specifically, an increasing **excess gate voltage** $v_{GS}- V_t$ will result in a **higher channel conductivity** (in other words, a lower channel **resistivity**).

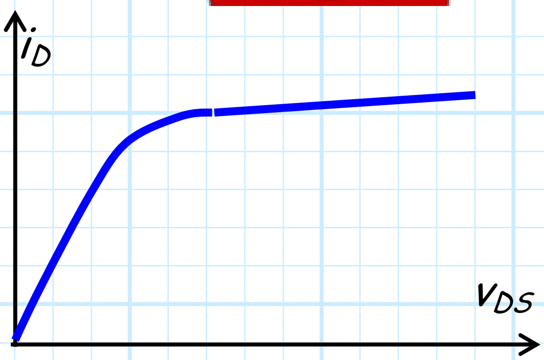
Thus, we find that the **drain current** i_D will **increase** as a positive **excess gate voltage** $v_{GS}- V_t$ **increases** (assuming that v_{DS} >0).

This process, of increasing the induced channel conductivity by increasing the excess gate voltage, is otherwise known as **channel enhancement**. This is where the **enhancement** MOSFET gets its name!

Q: *OK, but what about the relationship between drain current i_D and voltage v_{DS}?*



A: This relationship is a little **complicated**! Generally speaking, however, a **positive** v_{DS} results in a **positive** i_D, and the **larger** the v_{DS}, the **larger** the drain current i_D.



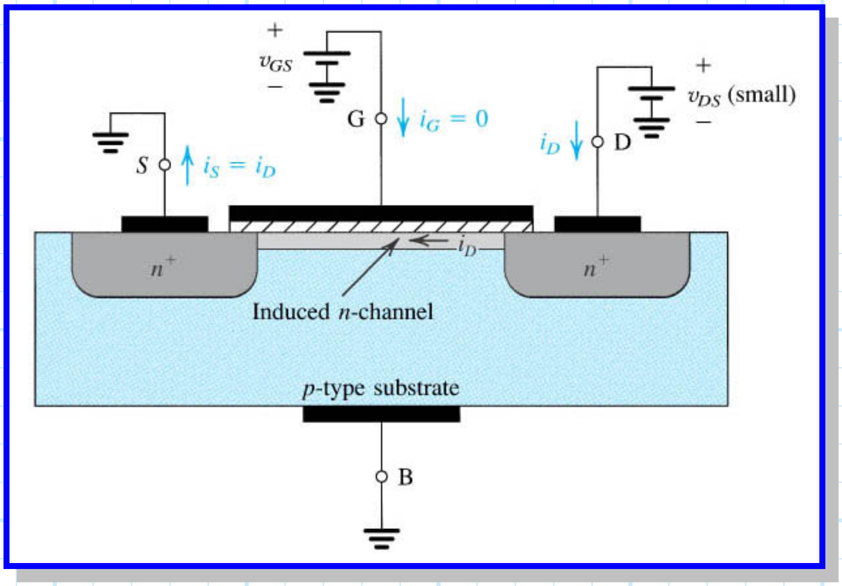
More specifically, we find that when v_{DS} is **small** (we'll see how small later), the drain current will be **directly proportional** to the voltage drain to source v_{DS}.

$$i_D \propto v_{DS} \quad \textbf{if } v_{DS} \text{ small}$$

In other words, if v_{DS} is **zero**, the drain current i_D is **zero**. Or, if the voltage v_{DS} **increases** by 10%, the drain current will likewise **increase** by 10%. Note this is **just like a resistor**!

$$i = \frac{v}{R} \qquad \therefore \; i \propto v$$

Thus, **if** (and **only** if!) v_{DS} is small, the induced channel behaves **like a resistor**—the current through the channel (i_D) is **directly proportional** to the voltage across it (v_{DS}).

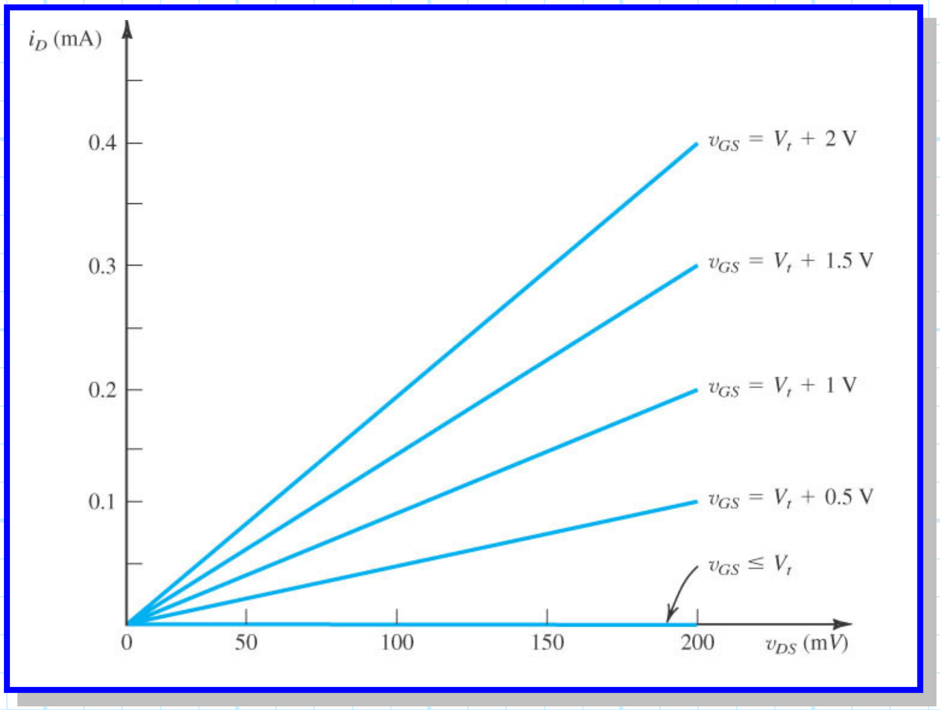


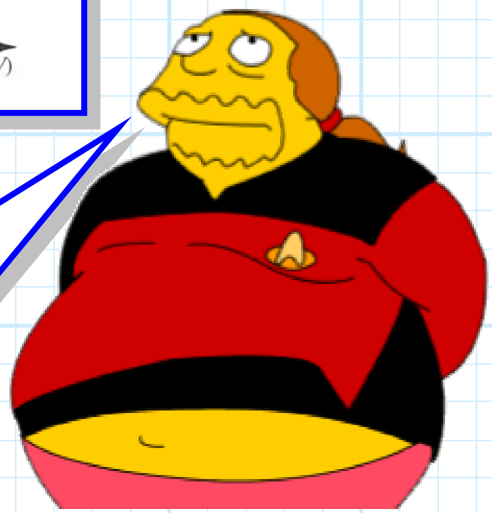
In other words, we can (for small values of v_{DS}), define a **channel resistance** r_{DS}:

$$\text{Since} \quad i_D \propto v_{DS}, \quad \frac{v_{DS}}{i_D} \doteq r_{DS} \quad \textbf{(if } v_{DS} \text{ small)}$$

Note that this resistance value depends on the **conductivity** of the induced channel—which in turn is dependent on the **excess gate voltage**!

Thus, if we were to **plot** drain current i_D versus v_{DS} for various excess gate voltages, we would see something like this:





Q: *Yawn! It is apparent that an NMOS transistor is so* ***simple*** *that virtually any intergalactic traveler should be able to understand it. It's just a* ***voltage controlled resistor****—right?*

A: WRONG! Remember, channel resistance r_{DS} **only** has meaning if v_{DS} is **small**—and most often v_{DS} will **not** be small!

As v_{DS} **increases** from our presumably small value, we find that **strange things** start to happen in our **channel**!

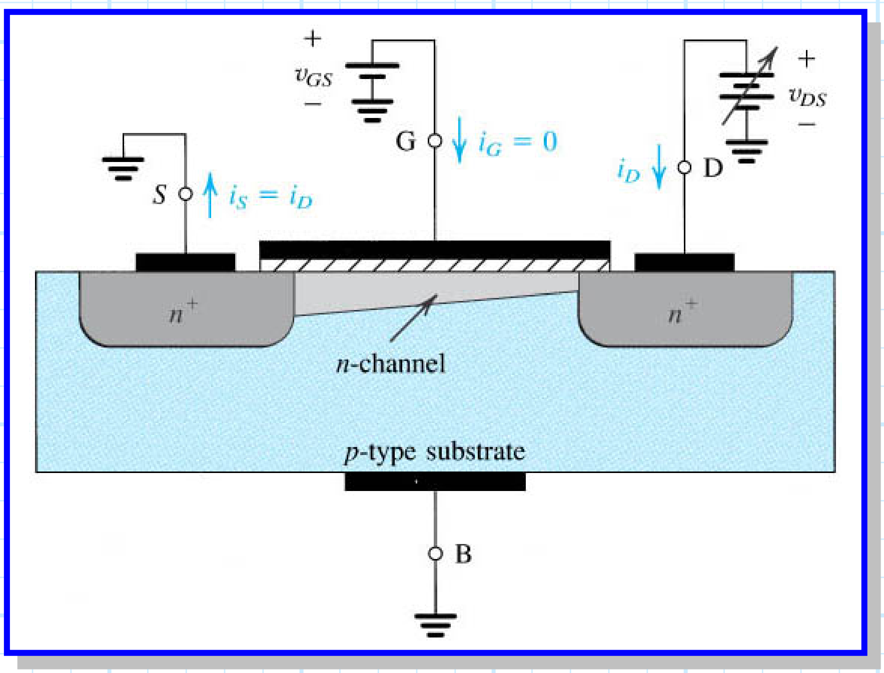
Recall that primarily, the **free-electrons** in our inversion layer (the induced channel) were attracted to the **gate** from the heavily doped **n+ Silicon** regions under the **drain** and source.

But the **gate** now has **competition** in attracting these free electrons!

It was "easy" to attract free electrons to the gate when the **gate electrode voltage** was much **larger** than both the drain and source voltage (i.e., when $v_{GS} \gg v_{DS}$). But as the **drain** voltage increases, it begins to attract **free electrons** of its **own**!

Recall that **positive current entering** the drain will actually consist mainly of **free electrons exiting** the drain! As a result, the **concentration** of free-electrons in our inversion layer will begin to **decrease** in the vicinity of the **drain**.

In other words, **increasing** v_{DS} will result in **decreasing** channel **conductivity**!

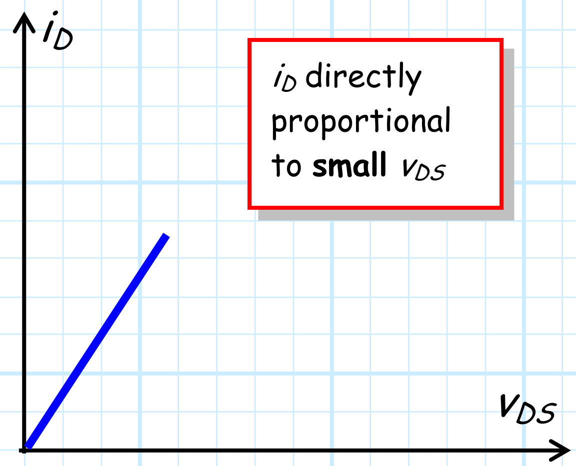


Thus, increasing the v_{DS} will have **two effects** on the NMOS device:

1. Increasing v_{DS} will **increase the potential difference** (voltage) across the conducting channel, an effect that works to **increase** the drain current i_D

2. Increasing v_{DS} will **decrease the conductivity** of the induced channel, and effect that works to **decrease** the drain current i_D.

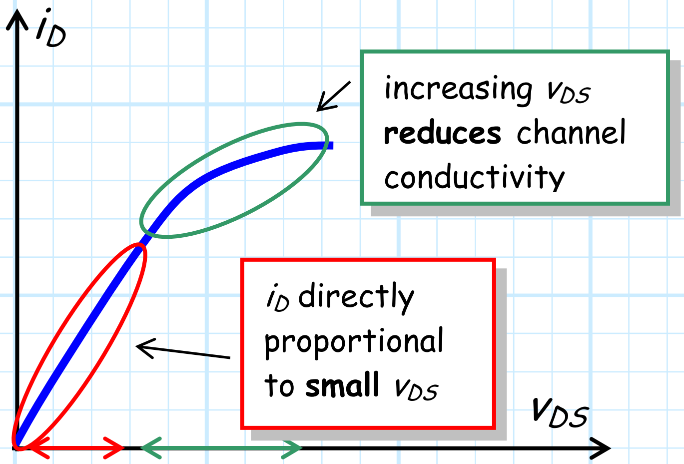
For **small** values of v_{DS}, the second effect is **tiny**, so that the increase in drain current is directly **proportional** to the increase in voltage v_{DS} (hence, we can define channel **resistance** r_{DS}). For example, a **10% increase** in v_{DS} will result in a **10% increase** in drain current.



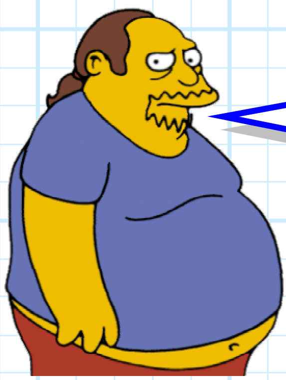
However, as v_{DS} increases, the **second effect** will become more and **more pronounced**. We find then that the drain current will **no longer** be directly **proportional** to the voltage v_{DS}. The reduction in channel conductivity will begin to "**counteract**" the increase in potential across the channel.

For example, a **10% increase** in v_{DS} may result in only a **9% increase** in i_D. Likewise, if we increase v_{DS} another 10%, the drain current may then increase **only 8%** (and so on).

Eventually, we find that the an increase in v_{DS} will result in **no** further increase drain current i_D!! Effect 2 will **completely** "counteract" effect 1, so that there is **no more** increase in drain current as v_{DS} increases.

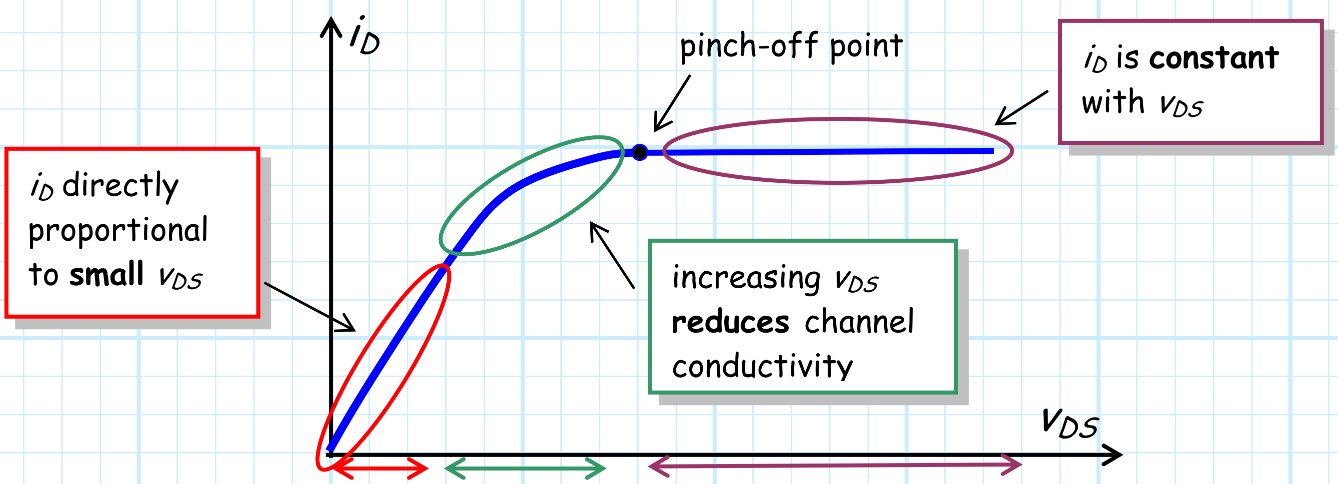


When this occurs, we say that we have "**pinched-off**" the induced channel—in other words the **channel is in pinch off**.



Q: *So, if we* ***continue*** *to increase v_{DS} after the channel is "**pinched off**", does the drain current actually begin to* ***decrease****?*

A: **NO!** A **interesting** thing happens when the channel is in pinch off. As we further increase v_{DS}, the drain current i_D will remain **unchanged** (approximately)! That is, the drain current will be a **constant** (approximately) with respect to v_{DS}.



Note that there are **three distinct channel conditions** in for NMOS operation.

* Depending on the value of v_{GS}, we can have an **induced channel**, or **no** conducting channel at all!

* Then **if** we have an **induced channel** (i.e.,$v_{GS} - V_t > 0$), (depending on the value of v_{DS}) the channel can be either be **pinched-off** or **not**!

Each of these **three** possibilities has a **name**—they are the names of our **NMOS transistor modes**!

1. **Cutoff** - When $v_{GS} - V_t < 0$, **no** channel is induced (no inversion layer is created), and so i_D=0. We call this mode **CUTOFF**.

2. **Triode** - When an induced channel **is** present (i.e., $v_{GS} - V_t > 0$), but the value of v_{DS} is **not** large enough to pinch-off this channel, the NMOS is said to be in **TRIODE** mode.

3. **Saturation** - When an induced channel **is** present (i.e., $v_{GS} - V_t > 0$), and the value of v_{DS} **is** large enough to pinch-off this channel, the NMOS is said to be in **SATURATION** mode.

We can **summarize** these modes in a table:

MODE	INDUCED CHANNEL?	CHANNEL PINCH-OFF?
CUTOFF	NO	N/A
TRIODE	YES	NO
SATURATION	YES	YES